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A Review - Synchronization Approaches to Digital systems

Sukanya. K*, Dr. G. Laxminarayana**
*(Department of E.C.E, TKR College of Engineering and Technology, Ranga Reddy, Telangana-500097)
**(Department of E.C.E, CVSR College of Engineering, Ranga Reddy, Telangana-501301)

ABSTRACT
Synchronization is a prime requirement in the process of Digital systems. Wherein new devices are upcoming towards providing higher service level, advanced distributed systems are been integrated onto a single platform for higher service provision. However with the integration of large processing units, the distributed processing needs a high level synchronization with minimum processing overhead. The issue of synchronization was processed by various approaches. This paper outlines a brief review on the developments made in the field of synchronization approach to digital system, under distributed mode operation.
***Keywords*:** Digital system, Distributed system, Processing overhead, Service level, Synchronization

I. INTRODUCTION

The demand of service over different applications has lead to the development of new devices with high speed processing. The systems are being designed with distributed processing unit, operating in parallel to provide faster computation. However the upcoming services are demanding for high processing efficiency and parallel processing of multiple operations. To cope up with the current demand and future demands, new processing architectures with multiple cores, distributed processing or pipelining process are emerging. With such high level processing, issue of synchronization among various sub-components exist. Hence, an architectural improvement would not satisfy the current and up-coming processing demands. To provide synchronization in an efficient manner, new synchronization approaches with pipelining, and distributed processing is required. Towards optimizing the processing efficiency, the processing digital system efficiency is measured in term of energy consumption, speed of operation and accuracy of operation. Wherein various approaches were developed to achieve these fundamental issues, a hybrid model of data and clock signaling was developed in past termed as 'Mesochronous processing'. In such coding, the data and clock signals were simultaneously communicated over the processing units to achieve synchronous operation. Wherein Mesochronous communication is benefited with synchronous processing, the efficiency of synchronous coding is required.

II. PREVIOUS METHODS

In the digital systems, synchronization has become an essential part. Towards optimizing synchronization problem with efficiency, various past approaches were made. These approaches are briefly reviewed in this paper. The approach of synchronization in the approach of processing, register optimization, circuit and architectural optimization, multiple core parallelizations, and its application to various fields such as network synchronization and communication synchronization is presented. The proper synchronization techniques will improve the power saving along with data processing speed.

a) Processing Approaches

A Mesochronous pipelining approach for pipelining process is suggested is presented in [1]. The clock period in conventional pipeline scheme is observed to be proportional to the maximum stage delay, whereas in a mesochronous pipelining it is proportional to the maximum delay difference, which leads to higher clock speeds in Mesochronous coding. The clock distribution is simpler hence leading to lower load and improves power saving. In [2], a new design methodology of digital system, called data-oriented methodology, to deal with the synchronization problems, by using Blue spec System was defined. Instead of conventional timing control mechanism, the data-oriented methodology adopts simple handshaking protocol, blocking transferring, and explicitly register/FIFO declaration for communicating between adjacent modules. In [3], a novel approach for parallelization of two-dimensional (2D) finite discrete element method (FDEM), aiming at clusters and desktop computers is developed. Dynamic domain decomposition based parallelization solvers covering all aspects of FDEM have been developed. The overall performance and scalability of the parallel code is been evaluated numerically and the suitability of the proposed approach is presented. In [4], a mergesoft and sample sorting approach is proposed. The suggested approach provides a mapping based on integer linear

programming to address load balancing and latency considerations. The suggested approach describes a prototype implementation of proposed approach for its runtime feasibility requirement. In [5], an idealized mesoscale simulation for multi processing unit is proposed. Good scalability is observed up to 49K processors in such system. Timing breakdown of computational tasks are determined with relocation of Lagrangian particles and interpolation of those particles to the grid identified as the most expensive operation and ideal for optimization. In [6], towards parallelization a heterogeneous compute kernels and predicting performance of the compilation results was suggested. In [7], a new intermediate format called unrolled concurrent control-flow graph with surface and depth to represent the structure of an Esterel program in pipelined computing is proposed. In [8] a mesochronous pipeline scheme is described operating on only one data set at a time. In this mesochronous scheme, pipeline stages operate on multiple data sets simultaneously. The variations in supply current drawn by clock network is significantly less in mesochronous scheme, thus power supply noise is observed to be less. In most of the digital systems the clock skew decreases the performance of the digital systems in terms of providing good sensitivity or to maintain data synchronization. In the conventional pipeline system facing problems due to improper synchronization of clock pulses. In [9], a universal problem observed in all digital systems called jitter or skew was focused. The propagation of information in the digital systems mainly controlled on the basis of clock pulses. In most of the digital systems the clock skew decreases the performance of the digital systems. A new system is implemented in the path of the clock to reduce the clock skew. In [10], a low complexity link micro architecture for mesochronous on-chip communication that enables skew constraint looseness in the clock tree synthesis, frequency speedup, power consumption reduction, and faster back-end turnarounds is proposed. In [11] a regular synchronizer and six multi synchronous synchronizers are implemented on a programmable logic device and the synchronization is measured. An experiment system and method for measuring synchronizers and metastable flip-flops are described. Two separate settling time constants are shown for a metastable flop. Clocking cross-talk between asynchronous clocks is demonstrated. A regular synchronizer useful for communications between asynchronous clock domains, while the other synchronizers providing higher bandwidth communications between multi-synchronous and mesochronous domains is presented. In [12] a work on Synchronous Digital Hierarchy is reviewed. A brief review regarding the problems in synchronization of different data rate signals in single clock, and master slave technique overcome the issue of synchronization problem. In [13] a low complexity link micro architecture for mesochronous on-chip communication that enables skew constraint looseness in the clock tree synthesis, frequency speedup, power consumption reduction, and faster back-end turnarounds is proposed. With respect to the state of the art, the proposed link architecture stands for its low power and low complexity overheads. Moreover, it can be easily integrated into a conventional digital design flow since it is implemented by means of standard cells only. In [14] a short tutorial attempts to present the approach and the criticality of the subject of metastability and synchronizers is presented. The issue with system metastability for false operation is proposed. In [15] for generating sequential code, the concurrency expressed in the synchronous programs is sequentialized. The developed approach was designed to run on single-core processors. An attempt generating multi-threaded code from polychronous data-flow model is proposed. In [16] an approach of synchrony conditions for purely asynchronous model in a way that avoids any reference to message delays and computing step times, as well as system-wide constraints on execution patterns and network topology is proposed. A Asynchronous Bounded-Cycle (ABC) model just bounds the ratio of the number of forward and backward-oriented messages in certain relevant cycles in the space–time diagram of an asynchronous execution is proposed. The clock synchronization and lock-step rounds is implemented and proved for the suggested ABC model.

b) Register Optimization approach

In [17] for synchronization in a breadth search approach, a fine grain processing for synchronization issue is developed. The data locality in this system is evaluated. A codelet model focusing on the fine grain parallelism of processing in synchronous mode is proposed. The Codelet Model more efficiently exploits data locality than the Open MP-like execution models which traditionally focus on coarse-grain parallelism inside loops. In [18], a high level implementation of L1-Cache system based on asynchronous communication oriented design style is proposed. Each of the units of cache architecture is pipelined asynchronously using asynchronous interfaces. The enhanced pipelining increases the area and energy resulting to the increased control circuitry requirement for handling large number of handshakes, resulting in saving of considerable area omitting clock generation, distribution and gating circuitry. The developments on the architectural level developments were reviewed and the future development towards the synchronization requirement is presented in [19]. Due to the fact that each cache memory implementation is time

consuming and error prone process, a synthesizable and a configurable model proves out to be of immense help as it aids in generating a range of caches in a reproducible and quick fashion. The micro pipelined cache, implemented using C-Elements acts as a distributed message-passing system. The RTL cache model implemented, comprising of data and instruction caches which has a wide array of configurable parameters. In addition to timing robustness this implementation has high average cache throughput and low latency. The implemented architecture comprises of two direct-mapped, write-through caches for data and instruction.

c) Multiple core parallelization

In [20], focus on two different kinds of parallel desktop architectures: multicore processors and GPU accelerators was made. The GPU implementation was carried out based on compute unified device architecture, while the multicore implementation was realized using open multiprocessing. The parallel performance and energy consumption were compared in the context of a quantitative remote sensing retrieval application. In [21], a multi core architecture following parallel processing is developed. The limitation of the multi core aware programs are analyzed, and at the same time, parallel programming issues are presented. It is focused to develop a method with little latency and synchronization overheads, for which a loose synchronization mechanism called "weak synchronization" is outlined. [22] explores the concepts of multi-core, trending research areas in the field of multi-core processors and then concentrates on power management issues in multi-core architectures.

In [23], a novel scheduling algorithm for pipelines streaming applications onto multi/many core architectures is presented. The algorithm generates pipeline schedules by formulating and solving MILP (Mixed Integer Linear Programming) problems. The suggested approach generates schedules that use up to 71% smaller amount of buffers needed for communication between kernels compared to conventional approaches. In [24], an architectural design of a six-way VLIW digital signal processor (DSP) with clustered register files was proposed. The architecture was designed for a variable length instruction set and supporting dynamic instruction dispatching. The one-level memory system architecture of the processor instruction and data caches and with instruction and data on-chip RAM was proposed.

d) Applications to Network synchronization

The synchronization in network on chip, a mesochronous scheme for communication over serial buses in network on chips (NoC) is proposed in [25]. The technique, which removes metastability errors in mesochronous communications, makes use of only one strobe line with the bus is defined. The strobe line toggles once with every frame of the data. In the suggested method, the frequencies of the transmitter and the receiver are kept independent. In [26], a switch design which greatly reduces the overhead for mesochronous synchronization and different layout constraints is proposed. A framework of mesochronous links that can direct the selection of synchronization options on a port by- port basis for all the switches in the NoC, based on timing and layout constraints is proposed. In [27], a scheme to handle mesochronous communication in NoC is presented. The proposed approach analyzes (i) the circuit design, (ii) the timing properties, (iii) the requirements to support flow control across mesochronous links, (iv) the implementation cost of such a scheme after placement and routing is proposed. In [28], two high-throughput, low-latency converters which could be used to convert synchronous communication protocol to asynchronous one and vice versa is proposed. The two hardware components have been designed to use in Multi-Processor System on Chip communicating by a full asynchronous Network on Chip (NoC). The proposed architecture was made generic, which allows the system designer to make various trade-off between latency and robustness, depending on the selected synchronizer. In [29], a run-time environment that supports classes of programming models and their composition for synchronization in network processor was presented. This approach combines the single-process multi-threaded execution inside the compute clusters and I/O subsystems, with set of specific Inter-Process Communication (IPC) primitives that exploit the NoC architecture. This approach provides a run-time support for the different target programming models in multi-process environment. In [30], a low-power, high-speed source-synchronous link transceiver was proposed. The techniques for NoC applications for power optimization in relate to synchronization is proposed. The issue of random mismatch, crosstalk, and different count of transceiver unit in the network is suggested. In [31], focus on NP-based high performance inline stateful deep inspection is made. This approach provides a dominant function block in intrusion prevention systems (IPSs). This approach investigates architecture-aware session design on NPs, and provides an instance of implementation to exploit the parallelism of the multi-core, multithreaded NP. In [32], stateful pipeline buffers added to long links allowing higher clock rate. The wastage of resources on links needing only low bandwidth was focused. In the asynchronous NoCs, link pipelining is applied only to those that will benefit from both increased through-put and

buffering capacity, and is especially useful in heterogeneous embedded SoCs. Two strategies that determine where link pipeline buffers should be placed in the topology is evaluated. The first compares available link bandwidth, based on physical wirelength, to the throughput needed by each source-to-destination path, for each link. In [33], a composable and predictable NoC architecture, that offers only GS, based on flit-synchronous Time Division Multiplexing (TDM) is proposed. In contrast to other TDM based NoCs, scalability on the physical level is achieved by using mesochronous or asynchronous links. Functional scalability is accomplished by completely isolating applications, and by having a router architecture that does not limit the number of service levels or connections.

e) Circuit and architectural optimization

In [34], a stencil computation for implementation of state-of-the-art general purpose graphics processing units is suggested. Stencil codes are used for the core of numerical solvers and physical simulation codes used for computing. The operation of stencil code used for their superior floating point performance and memory bandwidth is presented. Especially memory bound stencil codes were proposed exploiting the enlarged on-chip shared memory to perform two time step updates per sweep. This represents the application of temporal blocking for stencils on processing units. It has been presented a concise methodology to enable Invasive Programming properties on an embedded Multi-Processor System-on-Chip (MPSoC) in [35]. This is achieved by combining a designer-guided code parallelization approach with a virtualization, generic, and scalable embedded MPSoC architecture. To resolve data dependencies during task invasion, a processor-independent task-based communication scheme for the MPSoC is proposed. The approach is demonstrated by the generation of an MPSoC, featuring eight processors executing an application which dynamically switches at runtime between sequential and parallel execution. For the application applicability, and with the number of events used in [36], a multi-threaded CPU Open MP coding is proposed giving best performance under parallel processing. The study also shows that there is a "break-even" point of the number of events where the use of GPUs helps performance and improves computation time. In [37], a distributed clock generation scheme for Systems-on-Chip under variant fault condition was proposed. A self-stabilizing hardware blocks and a hybrid synchronous/asynchronous state machine enabling metastability-free transitions of the algorithm's states was proposed. In [38], a clock network design methodology that optimizes register placement was proposed. In the suggested work, for a given cell placement, incremental modifications are performed based on the clock skew specifications by moving registers toward preferred locations that may reduce the clock network size. At the same time, the side-effects to logic cell placement, such as signal net wire length and critical path delay, were controlled. In [39], a simple method using logic gates are taken to check the previous flip flop binary information. The logic gates create simple delay in producing the clock to the next stage. Until the logic gates identify the next binary bit from previous stage it will not allow the clock generator to pass the next clock pulse to the next stage of the circuit. In [40], an architecture called asynchronous array of simple processors (AsAP) is defined. AsAP uses a simple processor architecture with small memories to increase energy efficiency. The globally asynchronous locally synchronous **(**GALS) clocking style and nearest-neighbor communications improves the scalability, and provide opportunities to mitigate effects of device variations, global wire limitations, and processor failures. In [41], a new structure of a DLL circuit with clock alignment capability of both leading and trailing output pulse edges is defined. This circuit is used to obtain correct the duty-cycle factor in a multistage clock buffer operation. In [42], a transistor level modeling for delay tolerance logic was developed. The suggested approach avoids a significant increase in delay by allowing a full rail-to-rail swing on a lightly loaded second dynamic node with a small parasitic capacitance and which is inversely coupled to the output. In [43], parallel application signature for performance prediction (PAS2P) is proposed. Based on the application's message-passing activity, to identify and extract representative phases, with which a parallel application signature is created which enable to predict the application's performance under synchronous mode of communication is proposed. The approach experimented with different scientific applications on different clusters. In [44], several new design strategies, which represent the current design trends to deal with the emerging issues were explored. For recognizing the stringent requirements on power consumption, memory bandwidth/latency, and transistor variability, novel power/thermal management, multi-processor SoC, reconfigurable logic, and design for verification and testing have been incorporated into system design. In [45], analysis on cluster global time continuity, using global time change models for the node dynamics is proposed. The obtained results shown that defining the global time using the cluster average time (AGT) is more stable than defining it using a single node's local time (SGT). With normally distributed clock-parameter assumptions, the AGT change bounds are at most 70.7% of those for the SGT's. In [46], the impact of the Total Store Order (TSO) memory

model is investigated, which is used by Intel x86 and Sun SPARC processors, on secure information flow. Two approaches of data flow for information flow in such processor architecture is proposed. In [47], a methodology for the design and implementation of a self-timed reconfigurable control device suitable for a parallel cascaded flip-flop synchronizer based on a principle known as wagging, operating through the application of distributed feedback graphs is proposed. By modifying the endpoint adjacency of a common behavior graph via one-hot codes, several configurable modes can be implemented in a single design specification, thereby facilitating direct control over the synchronization time and the mean-time between failures of the parallel master-slave latches in the synchronizer. In [48], a Clock distribution networks is proposed which synchronize the flow of data signals among synchronous data paths. The designs of these networks dramatically affect system-wide performance and reliability. A theoretical background of clock skew is provided in order to better understand how clock distribution networks interact with data paths. Minimum and maximum timing constraints are developed from the relative timing between the localized clock skew and the data paths. These constraint relationships are reviewed, and compensating design techniques were discussed. In [49], an on-chip measurement circuit to measure multi-giga bit cycle-to-cycle jitter based on the vernier oscillator (VO) is proposed. This is inherited from the famous vernier delay line. The calibration of this method is also given. The circuit adopts a differential digital controlled delay element, which makes the circuit flexible in adjusting the measurement resolution, and a highly sensitive phase capturer, which makes the circuit able to measure jitters in pico-second range. In [50], a special purpose processing element is described which is used to optimize the operational outline of the processing element. It has been used to configure the FPGAs of the massively parallel hardware platform RIVYERA. In [51], a novel low power adaptive pulse triggered flip-flop (PTFF) featuring exclusive-or gate based clock gating with replica path delay scheme is proposed. Clock gating is a very accepted technique to reduce dynamic power of idle clocking subsystems. Incorporating clock gating with PTFF leads to reduction in dynamic power consumption and replica path delay pulse generator simplifies design effort and achieves robust timing characteristics as compared to the conventional PTFF. The proposed PTFF features best power delay product performance. In [52], to achieve the issue of synchronization, a technique for reducing the S/N ratio of emanating information by signal reduction and noise generation have been proposed. A technique that fluctuate frequencies of synchronizing signal to reduce correlation between timings of display and transmission is proposed. In [53], the phase-stabilized transfer of a chirped frequency as a tool for synchronization and time transfer is proposed. A remote measure for the synchronization of remote counters' gate intervals without using an external time reference is proposed. The results were directly applicable to the remote synchronization of frequency measurements. In [54], A robust, scalable, and power efficient dual-clock first-input first-out (FIFO) architecture which is useful for transferring data between modules operating in different clock domains is presented. The architecture supports correct operation in applications where multiple clock cycles of latency exist between the data producer, FIFO, and the data consumer; and with arbitrary clock frequency changes, halting, and restarting in one or both clock domains. In [55], a parallel computing demands synchronous clocking of multiple core processors to reliably carry out joint computations is proposed. The mutually coupled phase-locked loops (PLLs) enable synchronous clocking in large-scale systems with transmission delays. A phase description of coupled PLLs that includes filter kernels and delayed signal transmission is proposed. The transmission delays in the coupling, enable the existence of stable synchronized states, while instantaneously coupled PLLs do not tend to synchronize. The filtering and transmission delays combinly govern the collective frequency and the time scale of synchronization.

f) Communication application

In [56], an approach to timing and data handling that support the operation of single and correlated communication systems at their maximum capacity was proposed. The suggested approach was focused for FPGA device operating for higher operating frequency of operation. In [57], a novel lumped time-delay compensation scheme for an communication system was proposed. The transfer of data in the flow was synchronized with a time delay of different quantized pulse, accurately compensated with a simple structure compared to the multiple time-delay lines. In [58], a formal specification and verification of a new fault-tolerant real-time communication protocol, called *DoRiS*, is suggested. This approach is designed for supporting distributed real-time systems that use a shared high-bandwidth medium. In [59], certain value on the maximum number of messages communicated regardless of the sparsity pattern of the matrix is developed. The downside, however, is the increased message volume and the negligible redundant computation. Reducing the message latency costs at the expense of increasing message volume was suggested. Two iterative-improvement based on heuristics to alleviate the increase in the volume through one-to-one task-to-processor mapping is proposed. In [60], focuses on the

partitioning of transceiver systems and on the implementation of application-specific components to introduce an advanced multiprocessor system-on-chip interface and control architecture which is able to fulfill the requirements of future transceiver integrations is proposed. The proposed framework demonstrates a high degree of scalability, flexibility, and reusability. With the suggested approach the time to market for products can be reduced and fast adaptations to the requirements of the market are made feasible.

g) Globally asynchronous - Locally synchronous (GALS)

A novel burst-mode globally asynchronous - locally synchronous (GALS) technique was proposed in [61]. The goal of this technique was to improving the performance of the GALS approach for systems with predominantly bursty data transfer. The simulation results observed illustrated a significant performance improvement in comparison with the classical implementation of GALS using pausible clocking. In [62], the problem of synthesizing the asynchronous wrappers and glue logic needed for correct GALS implementation of a modular synchronous system is proposed. Suggested approach was developed based on the weakly endochronous synchronous model, which defines high-level, implementation-independent conditions guaranteeing correct de-synchronization at the level of the abstract synchronous model. In [63], a novel GALS architecture for a general-purpose multiprocessor platform that is intended specifically for the use in hard real-time systems is proposed. The platform contains one NoC offering access to a shared memory and one NoC supporting message passing, each of them optimized for its purpose of use is developed. A message passing NoC architecture and implementation reflecting two main requirements: 1) support for hard real-time applications and 2) implementation of GALS is developed. In [64], a Synchronizers and arbiters for any Globally Asynchronous, Locally Synchronous network is proposed. They contribute to latency, because of the synchronization time required for reliability, and to metastability delay in the arbiters. In [65], a clock distribution and synchronization approach to address the issue of jitter in large scale circuit is proposed. A reconfigurable data path processor (RDP) is proposed, which is carried out in several stages for synchronization. The operation of synchronization was carried over a operand routing network (ORN) and clock control, synchronization scheme.

III. CONCLUSION

Synchronization is observed to be a very important issue in digital systems. The approach of providing synchronization is variant. In this survey, it is illustrated that various modes of parallelization architectures and processing methods were developed. Various modes of register optimization methods were developed to minimize the delay latency issue in digital system operation. In the modeling of synchronization approach to SoC modeling the application to network synchronization was observed. In the current developments and future prospective new NoC units are developing, though the integration has various advantages, the processing synchronization and power consumptions are a major issue. In various real time applications this approach of global synchronization issue is to be solved for a better services. This observation leads to the requirement of synchronization in digital system designing, and its limitation in resource utilization in term of power and area coverage constraints.

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K. SUKANYA presently working as Associate professor in the department of Electronics and Communication Engineering at TKR College of Engineering & Technology, Medbowli, Meerpet, SaroorNagar, Hyderabad, Telangana State, INDIA. She has 7 years of teaching experience. She is associated with ISTE as life member. She has obtained B. Tech. degree in Electronics and Communication Engineering from Jayamukhi Institute of Technological Sciences, Warangal, Jawaharlal Nehru Technological University Hyderabad, in 2006, M.Tech. degree in Embedded Systems from Ramappa Engineering College, Warangal, Jawaharlal Nehru Technological University Hyderabad, in 2011 and my area of Research interest is Embedded Systems, Ph.D (ECE) from Jawaharlal Nehru Technological University, Hyderabad and it is my part of Research work.

Dr. G. LAXMINARAYANA presently working as Principal of Anurag College of Engineering. He has obtained BE from Osmania university, M.Tech from Indian Institute of Science, Bangalore and Ph.D from JNTUH under the guidance of Dr. K. Lalkishore (VC of JNTUA). He has 5 years of industrial experience and 30 years of teaching experience. He worked in Osmania University from 1979 to 1998. He worked as Head of the department, ECE at Sreenidhi Engineering College, VBIT and Aurora. He also worked as Director of Aurora Scientific Technological and Research Academy and Principal of Holy Mary Institute of Technology. He is an industrial consultant in instrumentation and worked in South Central Railways. He is associated with ***IETE for last 20 years*** and also member of IEEE, ISOI and ISTE. Presently he is an ***Executive Committee member*** in the present body of Hyderabad IETE chapter and ***R&D subcommittee chair at IETE Hyderabad***. He is supervising 12 Ph.D students and published various papers in International journals and reputated National journals.